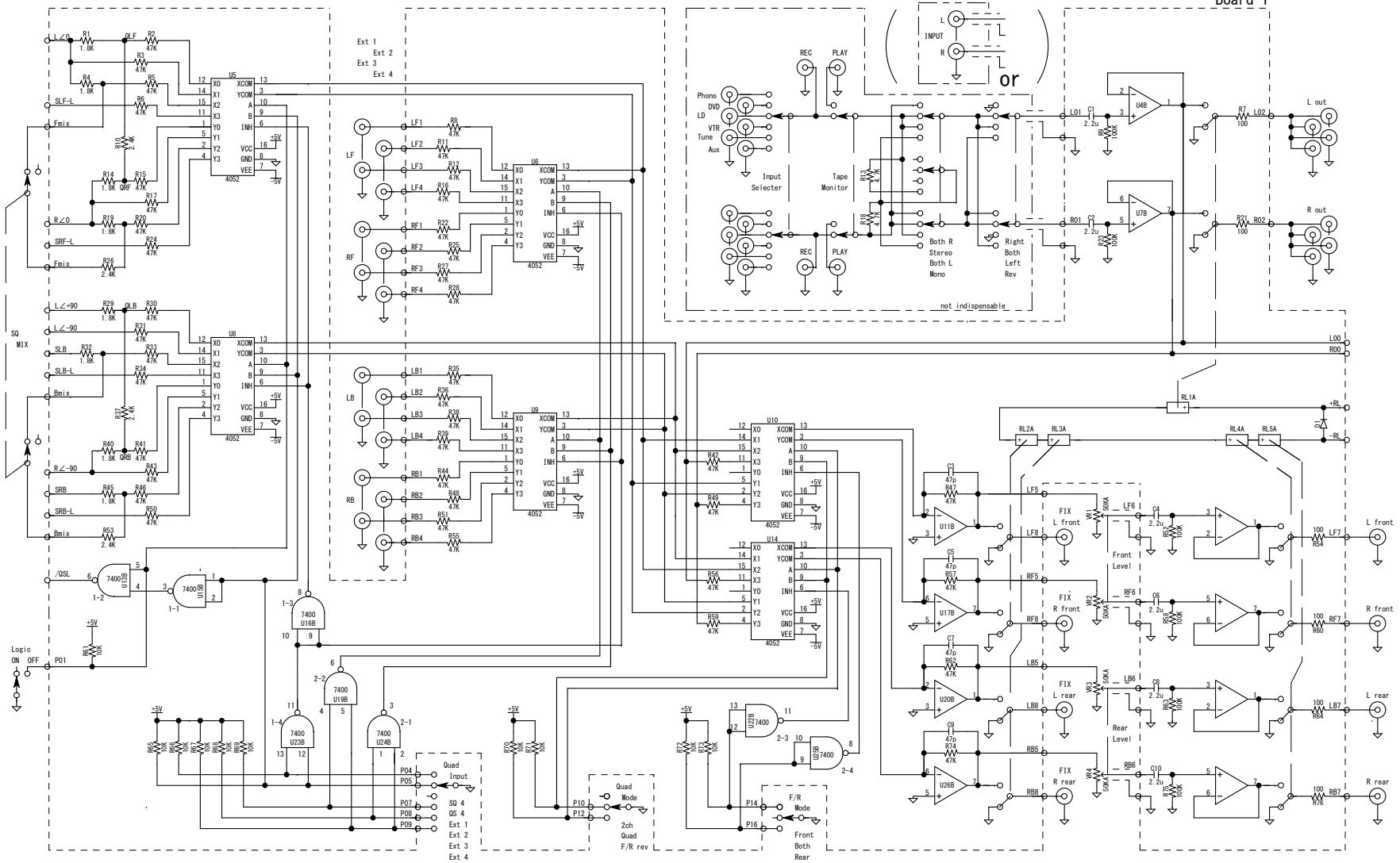
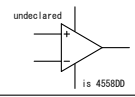


Board 1

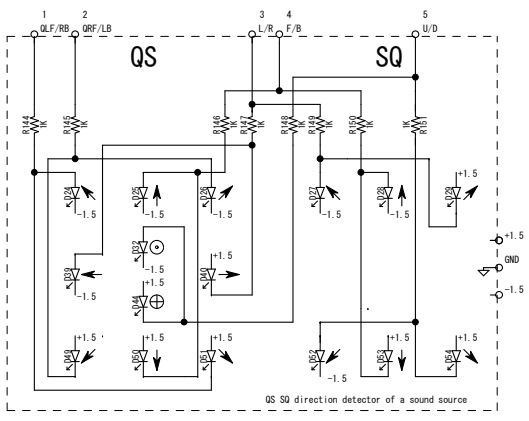
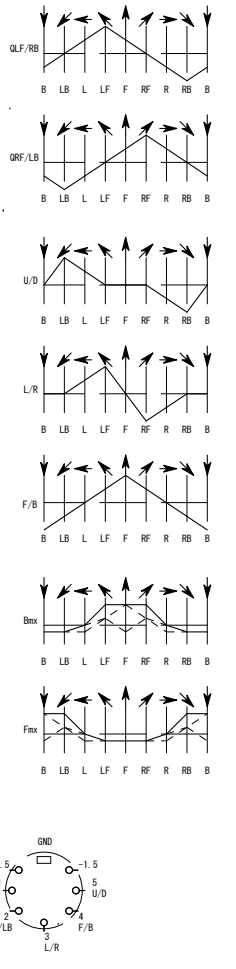
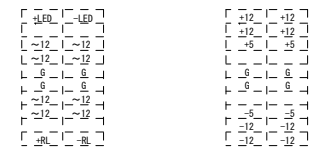
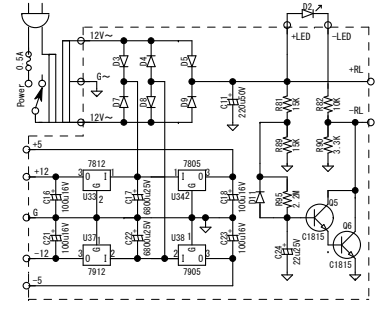
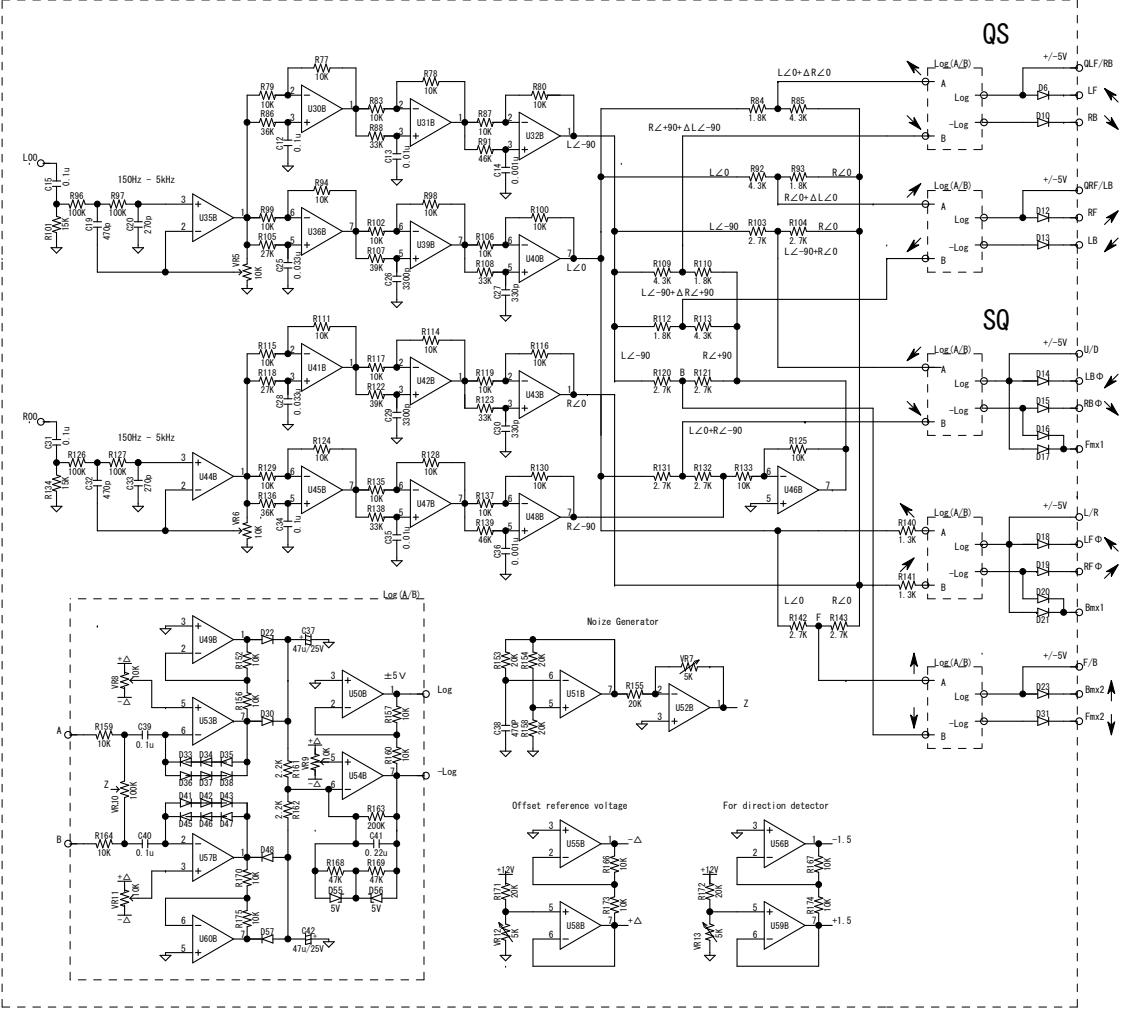


[ 2-8 ]	[ 6-9 ]	[ 2-10 ]	[ 2-1 ]	[ 2-2 ]	[ 2-3 ]	[ 2-4 ]	[ 2-5 ]	[ 2-6 ]	[ 2-7 ]
[ L01 ] [ G ]	[ /DSL ] [ G ]	[ Fmix ] [ G ]	[ LF1 ] [ G ]	[ LB1 ] [ G ]	[ +0.5 ] [ -0.5 ]	[ 12 ] [ 12 ]	[ LF ] [ G ]	[ LF5 ] [ G ]	[ +1.5 ] [ -1.5 ]
[ R01 ] [ G ]	[ /SL ] [ G ]	[ Bmix ] [ G ]	[ RF1 ] [ G ]	[ RB1 ] [ G ]	[ 0S 4 ] [ G ]	[ 12 ] [ 12 ]	[ RF ] [ G ]	[ RF5 ] [ G ]	[ 6 ] [ 6 ]
[ L02 ] [ G ]	[ L<90 ] [ G ]	[ G ] [ G ]	[ LF2 ] [ G ]	[ LB2 ] [ G ]	[ P01 ] [ P09 ]	[ 12 ] [ 12 ]	[ LB ] [ G ]	[ LB5 ] [ G ]	[ 6 ] [ 6 ]
[ R02 ] [ G ]	[ L<90 ] [ G ]	[ P04 ] [ P10 ]	[ RF2 ] [ G ]	[ RB2 ] [ G ]	[ P02 ] [ P08 ]	[ 12 ] [ 12 ]	[ LB ] [ G ]	[ LB5 ] [ G ]	[ 6 ] [ 6 ]
[ L00 ] [ G ]	[ R<90 ] [ G ]	[ P05 ] [ P12 ]	[ LF3 ] [ G ]	[ LB3 ] [ G ]	[ P03 ] [ P11 ]	[ 12 ] [ 12 ]	[ LB ] [ G ]	[ LB5 ] [ G ]	[ 6 ] [ 6 ]
[ R00 ] [ G ]	[ R<90 ] [ G ]	[ P06 ] [ P13 ]	[ RF3 ] [ G ]	[ RB3 ] [ G ]	[ P04 ] [ P10 ]	[ 12 ] [ 12 ]	[ LB ] [ G ]	[ LB5 ] [ G ]	[ 6 ] [ 6 ]
[ SLF-L ] [ G ]	[ /SL ] [ G ]	[ P07 ] [ P14 ]	[ LF4 ] [ G ]	[ LB4 ] [ G ]	[ P05 ] [ P11 ]	[ 12 ] [ 12 ]	[ LB ] [ G ]	[ LB5 ] [ G ]	[ 6 ] [ 6 ]
[ SRF-L ] [ G ]	[ /SR ] [ G ]	[ P08 ] [ P16 ]	[ RF4 ] [ G ]	[ RB4 ] [ G ]	[ P06 ] [ P12 ]	[ 12 ] [ 12 ]	[ LB ] [ G ]	[ LB5 ] [ G ]	[ 6 ] [ 6 ]
[ SLB-L ] [ G ]	[ /SL ] [ G ]	[ P09 ] [ P17 ]	[ LF5 ] [ G ]	[ LB5 ] [ G ]	[ P07 ] [ P13 ]	[ 12 ] [ 12 ]	[ LB ] [ G ]	[ LB5 ] [ G ]	[ 6 ] [ 6 ]
[ SRB-L ] [ G ]	[ /SR ] [ G ]	[ P10 ] [ P18 ]	[ RF5 ] [ G ]	[ RB5 ] [ G ]	[ P08 ] [ P14 ]	[ 12 ] [ 12 ]	[ LB ] [ G ]	[ LB5 ] [ G ]	[ 6 ] [ 6 ]

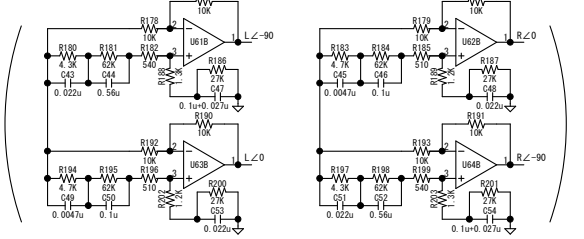


TITLE		DRAWING No.	
QS Logic / SQ Logic		4channel Decoder (sheet1-1)	
SHEET	DATE	DESIGN	
	2015/08/23		
			Fig. 13-1

Board 1



Simple phase Shifter ( Instead, Adjustment is difficult )

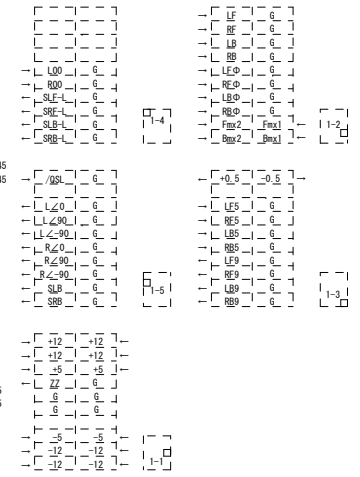
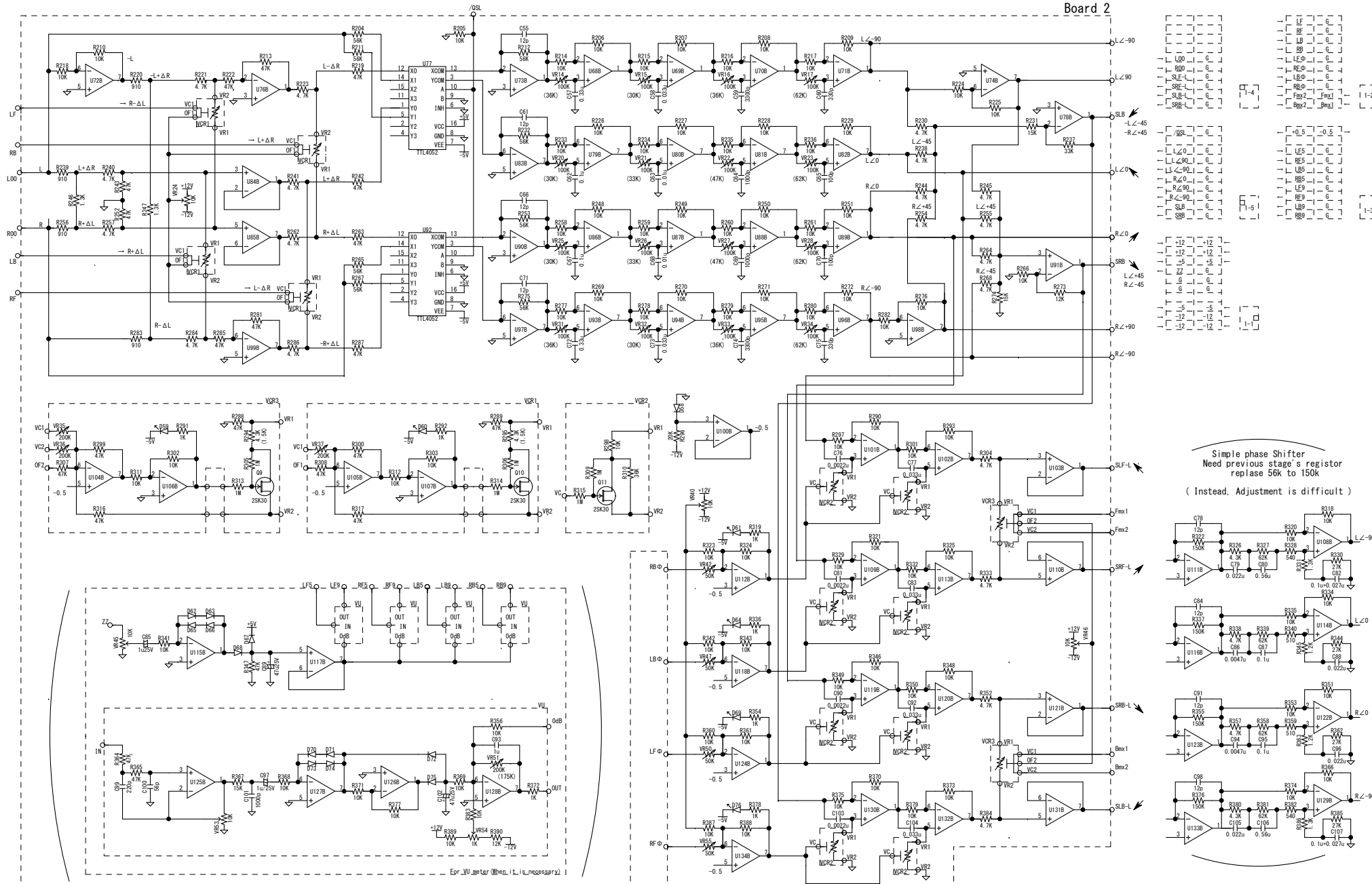


□ 2-8	□ 2-9	□ 2-10	□ 2-11	□ 2-12	□ 2-13	□ 2-14	□ 2-15	□ 2-16	□ 2-17	□ 2-18	□ 2-19	□ 2-20	□ 2-21	□ 2-22	□ 2-23	□ 2-24	□ 2-25	□ 2-26	□ 2-27	□ 2-28	□ 2-29	□ 2-30	□ 2-31	□ 2-32	□ 2-33	□ 2-34	□ 2-35	□ 2-36	□ 2-37	□ 2-38	□ 2-39	□ 2-40	□ 2-41	□ 2-42	□ 2-43	□ 2-44	□ 2-45	□ 2-46	□ 2-47	□ 2-48	□ 2-49	□ 2-50	□ 2-51	□ 2-52	□ 2-53	□ 2-54	□ 2-55	□ 2-56	□ 2-57	□ 2-58	□ 2-59	□ 2-60	□ 2-61	□ 2-62	□ 2-63	□ 2-64	□ 2-65	□ 2-66	□ 2-67	□ 2-68	□ 2-69	□ 2-70	□ 2-71	□ 2-72	□ 2-73	□ 2-74	□ 2-75	□ 2-76	□ 2-77	□ 2-78	□ 2-79	□ 2-80	□ 2-81	□ 2-82	□ 2-83	□ 2-84	□ 2-85	□ 2-86	□ 2-87	□ 2-88	□ 2-89	□ 2-90	□ 2-91	□ 2-92	□ 2-93	□ 2-94	□ 2-95	□ 2-96	□ 2-97	□ 2-98	□ 2-99	□ 2-100
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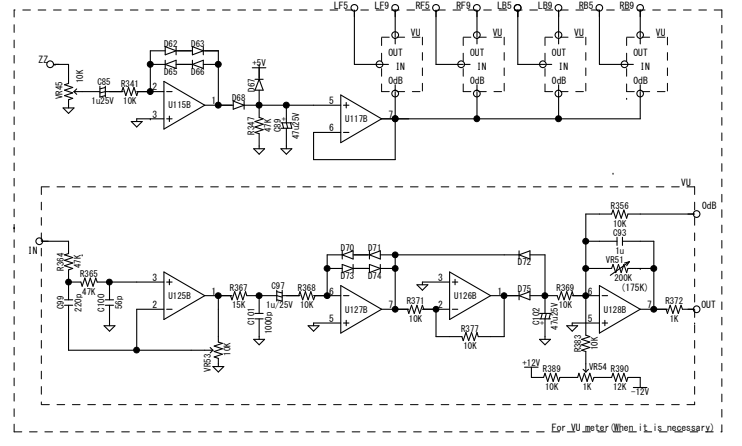
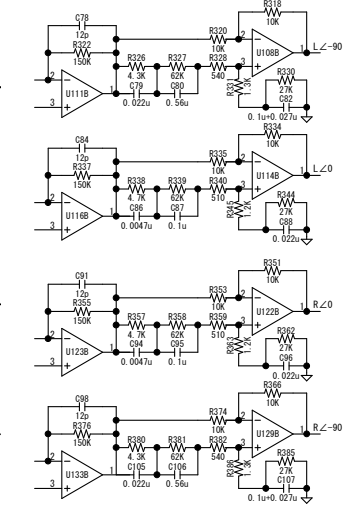
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DESIGN		DESIGN	
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TITLE		DRAWING No.	
SHEET		DATE	
DESIGN		DESIGN	
undecoded		is 455800	

Fig. 13-2

Board 2



Simple phase Shifter  
Need previous stage's register  
replase 56k to 150k  
( Instead, Adjustment is difficult )



TITLE		DRAWING No.	
		QS Logic / SQ Logic 4channel Decoder (sheet2)	
SHEET	DATE	DESIGN	
	2015/08/23		

